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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,972	12/03/2003	Jock F. Tomlinson	L00-010C1	5095

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LATTICE SEMICONDUCTOR CORPORATION
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EXAMINER

SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 11/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/726,972

Applicant(s)

TOMLINSON ET AL.

Examiner

Suresh K. Suryawanshi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/3/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-24 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 18-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants fail to describe having multiple power supplies for providing power to an electronic device in the provided specification or figures. Furthermore, figure 7 clearly discloses only one power supply 702.

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4. Claims 18-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicants fail to teach “a method of managing the providing of power from multiple power supplies to an electronic device”. Both figures and the specification fail to teach having multiple power supplies for providing power to an electronic device. Furthermore, figure 7 clearly discloses only one power supply 702. The examiner submits that it would require undue experimentation to make and use the claimed method of managing the providing of power from multiple power supplies to an electronic device.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8 and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Henze (US Patent No. 5,821,755).

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7. As per claim 1, Henze discloses a power management integrated circuit comprising:

a plurality of input terminals adapted to receive analog input voltage signals [Fig. 1; col. 3, lines 56-59; input terminals 14A and 14B];

a plurality of analog input monitor circuits coupled to the input terminals, each analog input monitor circuit operable to compare an input analog voltage received at an input terminal against at least one voltage reference [Fig. 1; col. 3, line 56 -- col. 4, line 8; comparators 46 and 48 and a voltage reference generator 52];

control logic coupled to the plurality of analog input monitor circuits and operable to generate at least one control signal in response to output signals from the analog input monitor circuits [Fig. 1; col. 4, lines 4-8; a control logic (flip-flop 60) outputs a control signal 62 in response to output signals from the comparators 46 and 48]; and

at least one driver circuit coupled between the control logic and an output terminal and capable of controlling a power switch, the drive circuit operable in response to a control signal from the control logic [Fig. 1; col. 4, lines 18-30; a power switch driver 64 controls the switching device 16 in response to the control signal 62 from the control logic 60].

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8. As per claim 2, Henze discloses that at least one analog input monitor circuit is operable to compare an input analog voltage against high and low voltage reference [Fig. 1; voltage reference generator 52].

9. As per claim 3, Henze discloses that at least one analog input monitor circuit is operable to compare a first input analog voltage received at a first input terminal to a second input analog voltage received at a second input terminal [Fig. 1; comparators 46 and 48].

10. As per claim 4, Henze discloses that at least one analog input monitor circuit is operable to monitor the voltage across an external resistor, and the control logic is operable to generate an indicator signal in response to the output signal from the analog input monitor circuit [Fig. 1; col. 4, lines 4-8; a control logic (flip-flop 60) outputs a control signal 62 in response to output signals from the comparators 46 and 48].

11. As per claim 5, Henze discloses that a programmable voltage reference generator [Fig. 1; voltage reference generator 52].

12. As per claim 8, Henze discloses that the control logic is programmable [Fig. 1].

13. As per claim 10, Henze discloses that the driver circuit is programmable [Fig. 1; power switch driver 64].

14. As per claim 11, Henze discloses that a charge pump circuit coupled to the driver circuit [inherent to a system having a driver circuit].

15. As per claim 12, Henze discloses that the driver circuit comprises an FET driver circuit capable of driving a power MOSFET switch coupled to the output terminal [Fig. 1].

16. As per claim 13, Henze discloses that a serial interface coupled to the control logic [inherent to the system as the control logic is connected to a power switch driver].

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 6-7 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent No. 5,821,755).

19. As per claim 16, Henze discloses a power management integrated circuit comprising:

at least one input terminal to receive an analog input voltage signal [Fig. 1; col. 3, lines 56-59; input terminals 14A and 14B];

at least one analog input monitor circuit coupled to the input terminal, the analog input monitor circuit operable to compare an input analog voltage received at the input terminal against at least one voltage reference [Fig. 1; col. 3, line 56 -- col. 4, line 8; comparators 46 and 48 and a voltage reference generator 52];

control logic coupled to the at least one input monitor circuit and operable to generate a plurality of control signals in response to an output signal from the at least one analog input monitor circuit [Fig. 1; col. 4, lines 4-8; a control logic (flip-flop 60) outputs a control signal 62 in response to output signals from the comparators 46 and 48]; and

a driver circuit coupled between the control logic and an output terminal and capable of controlling a power switch, each driver circuit operable in response to a control signal from the control logic [Fig. 1; col. 4, lines 18-30; a power switch driver 64 controls the switching device 16 in response to the control signal 62 from the control logic 60].

Henze does not expressly disclose about having a plurality of driver circuits. However, a routineer in the art would know how to implement the plurality of driver circuits by knowing how to implement a driver circuit as disclosed by Henze. In another words, a routineer in the art would be able to duplicate the disclosed driver circuit for a plurality of output terminals. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate the existing driver circuit as disclosed by Henze. Moreover, one would have a plurality of driver circuits in the case of having a plurality of output terminals where a driver circuit controls a corresponding output terminal.

20. As per claims 6-7 and 17, Henze discloses that the control logic is operable to generate a control signal that operates a driver circuit [Fig. 1]. Henze does not disclose about having a plurality of driver circuits. However, a routineer in the art would know how to implement the plurality of driver circuits by knowing how to implement a driver circuit as disclosed by Henze. In another words, a routineer in the art would be able to duplicate the disclosed driver circuit for a plurality of output terminals. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate the existing driver circuit as disclosed by Henze. Moreover, one would have a plurality of driver circuits in the case of having a plurality of output terminals where a driver circuit controls a corresponding output terminal.

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21. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent No. 5,821,755) in view of Sharpe-Geisler et (US Patent No. 5,751,164; hereinafter Sharpe).

22. As per claim 9, Henze discloses the invention substantially. Henze does not disclose about the control logic including a plurality of macrocells. However, Sharpe clearly discloses that use of macrocells in a complex programmable logic device is common [col. 2, lines 44-65] and a routineer in the art would know that a function as complex as a flip-flop can be implemented. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to power control of a device.

23. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent No. 5,821,755) in view of Kunz et al (US Patent No. 6,701,442 B1; hereinafter Kunz).

24. As per claim 14, Henze discloses the invention substantially. Henze does not expressly disclose about a nonvolatile programmable memory. But a routineer in the art would know that it is common to have a memory to store power management configuration information or indication in a computer system to control the power. However, Kunz clearly discloses such a nonvolatile memory for storing power configuration [Fig 2, 3; NV Memory 150; col. 6, lines 18-24; col. 8, lines 13-16]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to power control and management in a computer system.

25. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent No. 5,821,755) in view of Little (US Patent No. 5,175,845).

26. As per claim 15, Henze discloses the invention substantially. Henze does not disclose about a watchdog timer coupled to the control logic. However, Little clearly discloses that a watchdog timer is well known in the art and it is used to force a circuit into a reset state [col. 6, lines 3-10; col. 14, lines 16-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to power control and management in a computer system. Moreover, a watchdog timer will enhance the power management circuit of Henze, as now there will be a timer to reset the circuit if the circuit does not respond in a predetermined time period. Thus, one can avoid the system hanging for an unknown period of time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

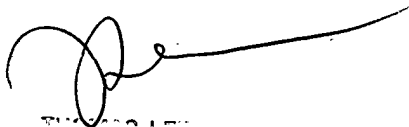
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

November 15, 2005



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SPECIAL AGENT IN CHARGE
TECHNICAL STAFF